REMARKS

The applicant thanks the examiner for discussing claim 1 and the Witt reference with the applicant's representatives, David L. Feigenbaum and Misha K. Hill, on September 14, 2005. The applicant pointed out why Witt is irrelevant to the claims based on arguments which are set forth below. The examiner generally conceded the applicant's position with respect to Witt. Amendments to claim 1 along the line of those made in this response were discussed.

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

> **5. Referring to claim 1, Witt has taught a method comprising in a processor which has a future file (Witt column 12, line 44; column 12 line 66 to column 13, line 7; and Figure 3) and which is capable of restoring the future file in a single clock cycle (Witt column 13, lines 40-46 and column 18, lines 54-67), restoring the future file over more than one clock cycle when a termination occurs in the processor (Witt column 19, lines 20-49).**

The applicant respectfully disagrees that Witt teaches a processor that is capable of restoring its future file in a single clock cycle, let alone that the processor restores the future file over more than one clock cycle. The cited passages of Witt make no mention of how many clock cycles are required to restore the future file. Witt mentions, at col. 18, ll. 65-67, that a "multi-ported structure may allow [a] future file 88 to be accessed, read from, and written to all in a single clock cycle," but this passage does not address how many cycles are used to restore the entire future file or any number of registers of the future file greater than one. Rather, it explains how an individual register may accessed more efficiently and makes no mention of how many cycles would be taken to restore more than one of such registers. Any inference that Witt would in fact restore more than one register of the future file in a single clock cycle is speculative.

In col. 19, ll. 20-39, Witt mentions that the future file is restored, but does not describe and would not have made obvious how many clock cycles are in fact used or that the number of clock cycles used is different than the number in which the processor is capable of restoring the

future file. There is nothing to support any inference about how many cycles are used, let alone that a different number is used than the examiner may have mistakenly inferred from col. 18's discussion of reading and writing in a single cycle.

Witt does not disclose and would not have made obvious a processor that restores "two or more registers of the future file over more than one clock cycle when a termination occurs in the processor" as in claim 1.

Independent claims 7 and 15 have been amended and are patentable for at least the reasons stated with respect to claim 1. Dependent claim 3 has been amended, and all of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, reference 10559-393001.

Respectfully submitted,

Date: 9/21/5

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